Amendments to the Claims:

Please cancel originally filed claims 1-39.

Please add the following new claims:

40. (new) A circuit for conditioning a digital pulse applied to an input thereof, said digital pulse characterized by having a predetermined minimum duration, said circuit comprising:

an input buffer, coupled to said input buffer and responsive to initiation of said digital pulse to initiate an output pulse on a buffer output terminal;

said input buffer having a control terminal for receiving a control signal;

control circuitry, coupled to said input buffer control terminal, for asserting said control signal in a predetermined timed relationship following initiation of said digital pulse;

said input buffer being responsive to assertion of said control signal to terminate said output pulse on said buffer output terminal;

wherein said output pulse has a duration shorter than said predetermined minimum duration of said digital pulse.

41. (new) A circuit in accordance with claim 40, wherein said output pulse has a duration of approximately three nanoseconds.

42. (new) A circuit in accordance with claim 40, implemented on a single integrated circuit.

43. (new) A circuit in accordance with claim 40, wherein said input buffer is implemented on a single integrated circuit, and said control circuit is disposed external of said integrated circuit.

44. (new) A circuit in accordance with claim 42, wherein said control signal is generated as a timed offset from an external clock signal.

45. (new) A circuit in accordance with claim 40, further comprising a disable circuit, coupled to said control circuit and to said input buffer control terminal, said disable circuit being responsive to assertion of an enable signal to prevent assertion of said control signal.

46. (new) A method for conditioning a digital pulse, said digital pulse characterized by having a predetermined minimum duration, said method comprising:

(a) initiating said digital pulse to the input of an input buffer, said input buffer being responsive to initiation of said digital pulse to initiate an output pulse on a buffer output terminal;

(b) asserting a control signal on a control input of said input buffer at a time relative to and subsequent to said initiation of said digital pulse;

(c) responsive to said assertion of said control signal, terminating said output pulse on said buffer terminal output terminal;

wherein said output pulse has a duration shorter than said predetermined minimum duration of said digital pulse.

47. (new) A method in accordance with claim 46, wherein said output pulse has a duration of approximately three nanoseconds.

48. (new) A method in accordance with claim 46, wherein said implemented on a single integrated circuit.

49. (new) A method in accordance with claim 46, wherein said input buffer is implemented on a single integrated circuit, and said control circuit is disposed external of said integrated circuit.

50. (new) A method in accordance with claim 48, futher comprising generating said control signal as a timed offset from an external clock signal.

51. (new) A method in accordance with claim 46, further comprising responding to assertion of an enable signal to prevent assertion of said control signal.

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